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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/981,624	10/16/2001	Anthony Debling	S1022/8760	7265
23628	7590	11/24/2004	EXAMINER	
WOLF GREENFIELD & SACKS, PC FEDERAL RESERVE PLAZA 600 ATLANTIC AVENUE BOSTON, MA 02210-2211			MCCARTHY, CHRISTOPHER S	
			ART UNIT	PAPER NUMBER
			2113	

DATE MAILED: 11/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/981,624	Applicant(s) DEBLING, ANTHONY	
	Examiner Christopher S. McCarthy	Art Unit 2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 October 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-4 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 16 October 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input checked="" type="checkbox"/> Other: <u>response to arguments</u> . |

DETAILED ACTION

1. Claims 1-4 are rejected under 35 U.S.C. 102(e) as being anticipated by Swoboda US2002/0059541, as cited in prior office action, which was mailed on 7/22/2004.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-4 are rejected under 35 U.S.C. 102(e) as being anticipated by Swoboda US2002/0059541.

As per claim 1, Swoboda teaches a debugging system comprising a host computer system and a target device (paragraph 0031), said target device having an embedded digital processor on an integrated circuit chip (paragraph 0069), an on-chip emulation device coupled to said digital processor (paragraph 0061, 0055), the on-chip emulation device being operable to control said digital processor and to collect information about the operation of said digital processor (paragraph 0061, 0038), the on-chip emulation device having a communication port operable to receive information from and emit information to the host computer system (paragraph 0080) wherein said debugging system further comprises an interface on said integrated circuit chip

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having a first port connected to said communication port of said on-chip emulation device (paragraph 0080) and a second port connected to a universal serial bus, said host computer system having a universal serial bus port connected to said universal serial bus (paragraph 0039) wherein said host computer system comprises a proxy server program for managing the universal serial bus port to enable communication over said universal serial bus, and said host computer further comprises application software in use communicating with the proxy server program and hence via said universal serial bus, with the or each digital processor (paragraph 0060, 0081, wherein, since more than one connection to the target can be utilized from the host, it is inherent that a proxy server be used as an intermediary to direct the various connections).

As per claim 2, Swoboda teaches the system of claim 1 wherein said target device has plural said embedded digital processors of said chip (paragraph 0082).

As per claim 3, Swoboda teaches a method of debugging an integrated circuit chip by communicating between application programs running on a host computer system and a device on said integrated circuit chip (paragraph 0031, 0060, 0038), the chip comprising digital processing circuitry (paragraph 0069) and on-chip emulation circuitry for communicating with and control of said digital processing circuitry (paragraph 0081), the on-chip emulation circuitry having a communications port for receiving information from said host computer system and for passing information to said host computer system (paragraph 0080), the integrated circuit chip further having an on-chip usb interface connected to a target usb port, and the host computer system having a host usb port (paragraph 0080, 0064, 0066), the method comprising: converting said host usb port to said target usb port (paragraph 0080, 0064, 0066); running a proxy server program on said host computer system, causing a said application program to connect to said

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proxy server program, whereby said proxy server program connects to said device on said chip via said host and target usb ports (paragraph 0039, 0060, 0081, wherein, since more than one connection to the target can be utilized from the host, it is inherent that a proxy server be used as an intermediary to direct the various connections).

As per claim 4, Swoboda teaches a method of operating an integrated circuit chip having digital processing circuitry and on-chip emulation circuitry for communicating with, and control of said digital processing circuitry (paragraph 0031, 0080, 0069), the on-chip emulation circuitry having a communications port for receiving information from a remote computer system and for passing information to said remote computer system (paragraph 0080), said integrated circuit chip further having an on-chip usb interface connected to a usb port (paragraph 0080, 0064, 0066), the method comprising converting said usb port to the usb port of a host computer (paragraph 0064, 0080, 0066), wherein said host computer is capable of Internet connection (paragraph 0064, 0066); running a proxy server process on said host computer (paragraph 0039, 0081, wherein, since more than one connection to the target can be utilized from the host, it is inherent that a proxy server be used as an intermediary to direct the various connections); generating a remote procedure call in said chip (paragraph 0061); transferring said remote procedure call via said usb to said proxy server process (paragraph 0061, 0039, 0064, 0066); converting said remote procedure call to a socket call (paragraph 0079, 0080, 0061); and thereby communicating between said chip and the Internet (paragraph 0064, 0080, 0065).

Response to Arguments

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4. Applicant's arguments filed 10/25/2004 have been fully considered but they are not persuasive.

Applicant has argued that Swoboda does not teach or suggest an integrated circuit chip comprising an embedded digital processor and an on-chip emulation device coupled to said digital processor. The examiner respectfully disagrees. The applicant is correct in his assertion that Swoboda utilizes an off-chip emulator controller, but as Swoboda clearly teaches in paragraph 0055, the emulator, as a whole, consists of four components. The last component taught is an "on-chip debug facility" (paragraph 0059). Since this debug facility is clearly on-chip and is an inclusive component of the emulator device, then an integral component of the emulator is on-chip and fulfills the limitation of an on-chip emulator. Therefore, all applicable rejected claims stand.

Applicant has also requested that a reference on a previous 1449 be reconsidered. The examiner requests that all pertinent information be disclosed as to the actual invention of the power debugger and not just a cover sheet declaring its availability.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period

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will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher S. McCarthy whose telephone number is (571)272-3651. The examiner can normally be reached on M-F, 9 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571)272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

csm
November 18, 2004


ROBERT BEAUSOLIEL
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100